REMARKS

In response to the above-identified Office Action, Applicant amends the application and seeks reconsideration thereof. In this response, Applicant amends claim 8. Applicant does not cancel or add any new claims. Accordingly, claims 8-10, 13-17 and 20-21 are pending.

I. Claims Rejected Under 35 U.S.C. §103(a)

The Patent Office rejects claims 8-10, 13-17, 20 and 21 under 35 U.S.C. 103(a) as being obvious over U.S. Patent No. 4,015,281 issued to Nagata et al. ("Nagata") in view of U.S. Patent No. 5,990,516 issued to Momose et al. ("Momose") and U.S. Patent No. 5,621,681 issued to Moon ("Moon"). Applicant amends claims 8 and 15.

Regarding the rejection of claim 8, among other elements, claim 8 defines a transistor device having a gate electrode overlying a gate dielectric formed directly on a semiconductor substrate comprising a first and second dielectric material being scalable for a set of feature size technologies, the set of feature size technologies defined by a gate length in the range of 25-70 nm wherein the first material thickness and second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$. According to the relationship, the sum of the thickness/dielectric constant of the first and second dielectric material must equal a thickness/dielectric constant for a gate dielectric of silicon dioxide. In making the rejection, the Patent Office characterizes Nagata as showing such a relationship at col. 4, lines 39-44. The cited formula, however, only provides an effective oxide thickness assuming one of the dielectric layers is silicon dioxide. The formula does not place limits, for example, on a thickness of a dielectric material based on the material's dielectric constant and a target thickness of silicon dioxide as the gate electrode. For example, rewriting the formula as a mathematical function to determine T_{SiO_2}/E_{SiO_2} would not give the same relationship as in claim 8.

The Patent Office characterizes Momose as showing "a semiconductor device having double layer gate dielectric in which the feature size technology has a gate length of 150 nm (or 0.15 μm) to form a high performance semiconductor having low power consumption." Paper No.20040405, page 3 (citing Momose, col. 16, lines 28-48 and col. 16, line 66 – col. 17, line 32).

The Patent Office further characterizes Momose as showing that the gate length can be decreased even more to improve the current drive capability and in one embodiment had a length of 40 nm. See Id., page 3 (citing Momose, col. 15, lines 13-31). In addition, the Patent Office alleges Momose shows one embodiment having a gate dielectric which is less than 1/3 the gate length. Momose does not provide any teaching about the thickness and type of material for a gate dielectric relative to a particular thickness for a gate dielectric of silicon dioxide.

Finally, Moon does not describe a device having a gate dielectric relationship relative to a particular thickness for a gate dielectric of silicon dioxide.

The failure of the combination of Nagata, Momose and Moon to teach or suggest each of the elements of claim 8 is fatal to the obviousness rejection. Therefore, claim 8 is not obvious over Nagata in view of Momose and Moon. Accordingly, Applicant respectfully requests withdrawal of the rejection of independent claim 8.

Claims 9-10 and 13-14 each depend from claim 8 and contain each of the elements thereof. Therefore, claims 9-10 and 13-14 are not obvious over Nagata in view of Momose and Moon at least for the same reasons as claim 8. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 9-10 and 13-14.

Regarding the rejection of claim 15, among other elements, claim 15 defines a semiconductor substrate having a transistor device formed thereon, the transistor device isolated from other devices by shallow trench structures and having a gate dielectric disposed directly between a surface of the substrate and a gate electrode comprising a first dielectric material selected from the group consisting of HfO_2, BaO, La_2O_3, Y_2O_3, and ZrO_2 and having a first dielectric constant and a second dielectric material having a second dielectric constant different from the first dielectric constant, the first and second dielectric materials being scalable for each of a plurality of feature size technologies, having a gate length in the range of 25-70 nm, and wherein the first material thickness and the second material thickness are determined by the relationship $t_1/k_1 + t_2/k_2 = t_{ox}/k_{ox}$ similar to claim 8. Therefore, Applicant respectfully submits the discussion above regarding the combination of Nagata, Momose and Moon failing to teach or suggest the relationship governing dielectric thickness and selection relative to a thickness of a gate dielectric

of silicon dioxide. Therefore, claim 15 is not obvious over Nagata in view of Momose and Moon. Accordingly, Applicant respectfully requests withdrawal of the rejection of claim 15.

Claims 16-17 and 20-21 depend from claim 15 and contain each of the elements thereof. Therefore, claims 16-17 and 20-21 are not obvious over Nagata in view of Momose and Moon at least for the same reasons as claim 15. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 16-17 and 20-21.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Patent Office believes that a telephone conference would be useful in moving the application forward to allowance, the Patent Office is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
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Dated: 10/26/04 By: William T Babbitt
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I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Nedy Calderon 10/26/04
Nedy Calderon Date